1. [10%] (a) Draw the logic diagram of SR latch with NOR gates, and (b) derive the function table of SR latch.

2. [30%] Derive the characteristic table, characteristic function and excitation table of (a) JK flip-flop, and (b) T flip-flop.

3. [20% (10/5/5)] A sequential circuit has one flip-flop $Q$, two inputs $x$ and $y$, and one output $S$. It consists of a full-adder circuit connected to a D flip-flop, as shown below. Derive the (a) state table, (b) state function $Q(t+1)$ and output function $S$, and (c) state diagram of the sequential function. (Problem 5-7)

4. [40%] Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6. Use JK flip-flops. Note: you must derive the (a) state diagram, (b) state table, (c) maps for input equations, and (d) logic diagram for the counter. (Problem 6-27)