1. [16% (8/8)] (a) Draw the logic diagram of D latch (with one control line C using four NAND gates), and (b) derive its function table. (Figure 5-6)

2. [24% (8/8/8)] Derive the (a) characteristic table, (b) characteristic function and (c) excitation table of T flip-flops. (Table 5-1; Page 178; Table 5-12b)

3. [10%] Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder. Use block diagrams for the components. (Problem 4-25)

4. [12% (6/6)] Implement the full adder with a 3x8 decoder. (a) Derive the truth table of the full adder and (b) draw the logic diagram. (Table 4-4, Figure 4-21)

5. [12% (6/6)] Implement the Boolean function with a multiplexer: \( F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15) \). (a) Derive the truth table and (b) draw the logic diagram (Problem 4-32)

6. [12% (6/6)] Design a BCD ripple counter using T flip-flops. (a) Derive the state diagram and (b) draw the logic diagram. (Figure 6-9, Figure 6-10)

7. [24% (6/6/6/6)] Design a 3-bit count-down counter in binary-coded decimal from 111 to 000 and back to 111. Use T flip-flops. Note: you must derive the (a) state diagram, (b) state table, (c) K-maps and (d) simplified input equations for the counter. (Similar to Page 236)