計算機組織　第一次小考

學號：　　姓名：

1. (15%)What components does an instruction set architecture contains?
   - A. Organization of programmable storage
     - (1) registers
     - (2) memory: flat, segmented
     - (3) Modes of addressing and accessing data items and instructions
   - B. Data types and data structures
     - (1) encoding and representation (next chapter)
   - C. Instruction formats
   - D. Instruction set (or operation code)
     - (1) ALU, control transfer, exceptional handling

2. (21%)Please illustrate the three kinds of instruction formats and give an MIPS assembly instruction example. Hint: fields in machine code

R: add $s0,$s1,$s2

I: lw $s1, 10($t1)　　beq $t4,$t5,Label

J: j 100

3. (21%) Convert -17.5 to IEEE single precision. Convert 510_{10} into 32-bit two's complement binary number. Convert 10.4_{10} to binary. Label bits clearly.

   1 1000 0011 0001 1000 0000 0000 0000 000

   0000 0000 00000 0000 0000 0001 1111 1110

   $10.4_{10} = 1010.\underline{0110}_2$

4. (14%)Please define overflow and underflow.

Overflow!

– A positive exponent becomes too large to fit in the exponent field

Underflow!

- A negative exponent becomes too large to fit in the exponent field

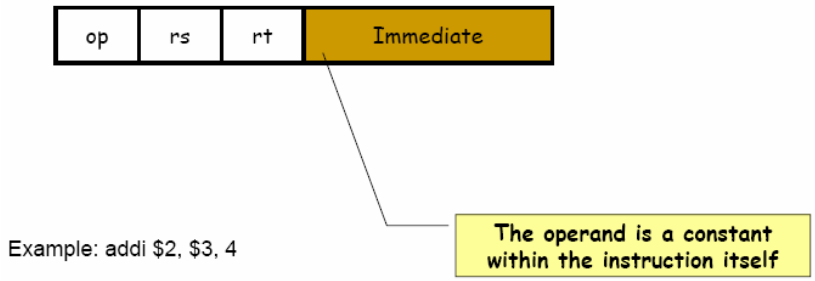
– (30%)MIPS has five addressing modes: immediate addressing, register addressing, base addressing, PC-relative addressing, and pseudo-direct addressing. Give their format and explain them.

Register	Add R4,R3	R4 ← R4+R3
Immediate	Add R4,#3	R4 ← R4+3
Displacement	Add R4,100(R1)	R4 ← R4+Mem[100+R1]
Register indirect	Add R4,(R1)	R4 ← R4+Mem[R1]

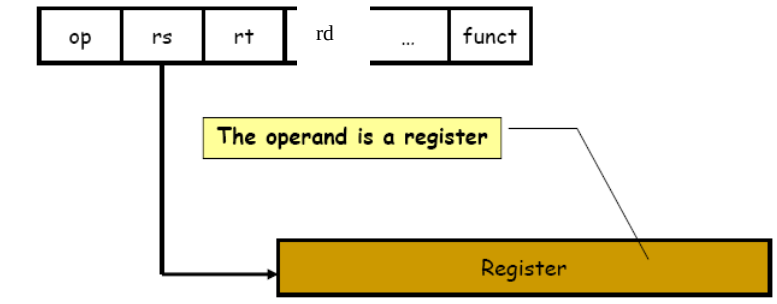
Pseudo-direct

畫圖，或是文字說明

- Immediate addressing

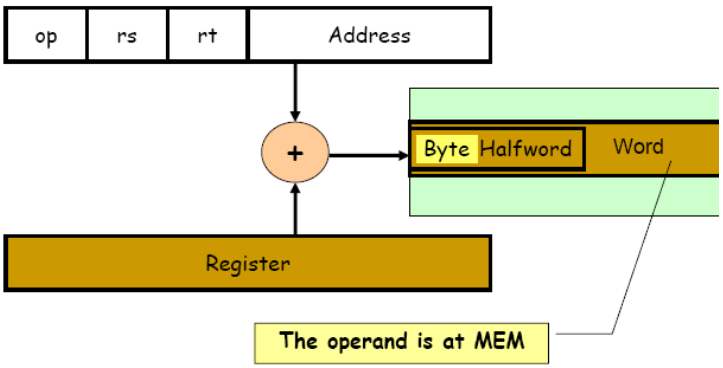


- Register addressing



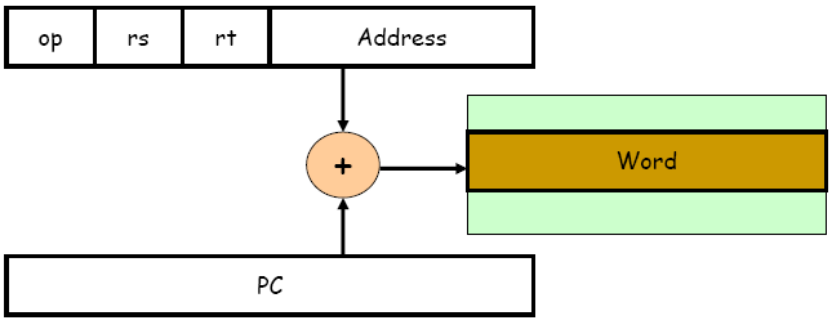
Example : add $r1, $r2, $r3

- Base addressing



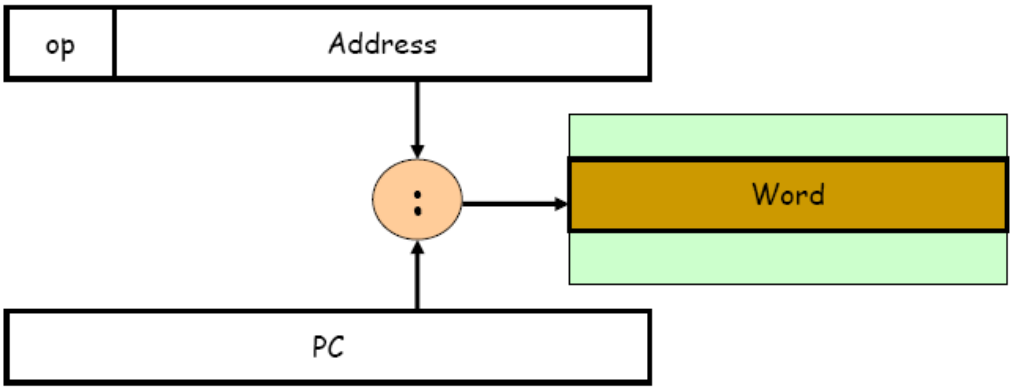
Example : lw $2, 100($3)

- PC-relative addressing



Example : beq $2, $3, 100

- Pseudodirect addressing



Example : j 100