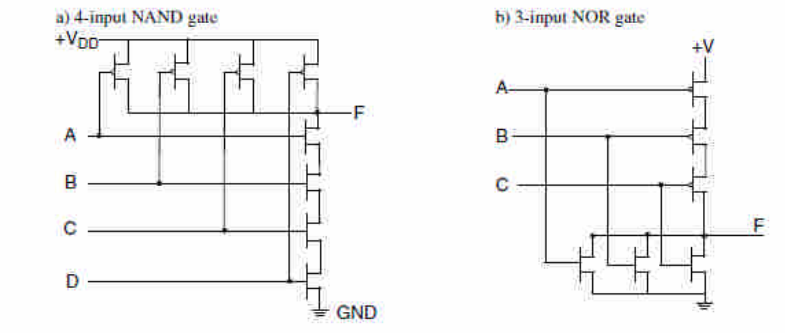
一００學年度第一學期 數位電路學 期中考試

範圍：Ch. 6~7　　上課教師：潘欣泰　　日期：100/12/8

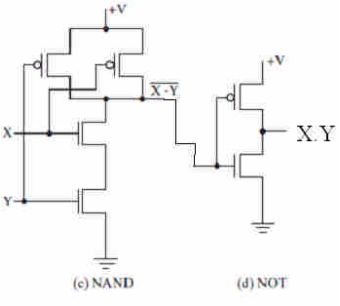
1. (20%) Find the CMOS switch model networks for the following functions:
   (1) 4-input NAND gate
   (2) 3-input NOR gate
   (3) 2-input AND gate

   Answer:

   (1), (2)



   (3) 2-input NAND + NOT



2. (20%) A sequential circuit is shown in Fig. 1. The timing parameters for the gates and flip-flops are as follows.

   Inverter: $t_{pd} = 0.02\,ns$

   XOR gate: $t_{pd} = 0.15\,ns$

   Flip-flop: $t_{pd} = 0.7\,ns$, $t_s = 0.2\,ns$, and $t_h = 0.1\,ns$

   (1) Find the longest path delay from an external circuit input passing through gates only to an external circuit output.
   (2) Find the longest path delay in the circuit from an external input to positive clock edge.
   (3) Find the longest path delay from positive clock edge to output.
   (4) Find the longest path delay from positive clock edge to positive clock edge.

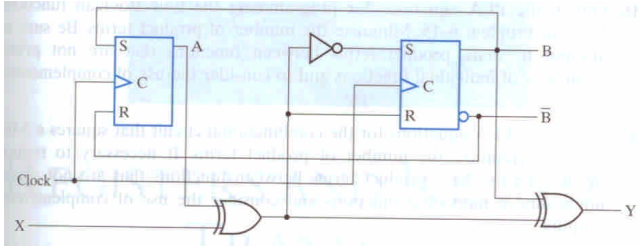


Fig. 1

Answer:

(1)2 × 0.15 (delay of XOR)= 0.3 ns

(2) $t_{pd}XOR + t_{pd}INV + t_{sFF} = 0.15 + 0.02 + 0.2 = 0.37ns$

(3) $t_{pd}FF + 2t_{pd}XOR = 0.7 + 2 \times 0.15 = 1\,ns$

(4) $t_{pd}FF + t_{pd}XOR + t_{pd}INV + t_sFF = 0.7 + 0.15 + 0.02 + 0.2 = 1.07ns$

3. (20%) Given the 16-bit operand 00111010 00110110, what operation must be performed and what operand must be used
   (1) to clear all odd bit positions to 0? (Assume bit positions are 15 through 0 from left to right)
   (2) to set leftmost 5 bits to 1?
   (3) to complement the most significant 8 bits?

   Answer:
   (1) AND with 0101 0101 0101 0101
   (2) OR with 1111 1000 0000 0000
   (3) XOR with 1111 1111 0000 0000

4. (20%) Use D-type flip-flops and gates to design a counter with the following repeated binary sequence: 0, 1, 4, 7.

   Answer:

present state			next state		
A	B	C	Da	Db	Dc
0	0	0	0	0	1
0	0	1	1	0	0
0	1	0	x	x	x
0	1	1	x	x	x
1	0	0	1	1	1
1	0	1	x	x	x
1	1	0	x	x	x
1	1	1	0	0	0

Da = AB' + B' C (or AB' + AC)
Db = AB' (or AC')
Dc = C'

5. (20%) A register cell is to be designed for an 8-bit register R0 that has the following register transfer functions:

$\overline{S1}\cdot\overline{S0}: R0 \leftarrow R0 \oplus R1$

$\overline{S1}\cdot S0: R0 \leftarrow R0 \vee R1$

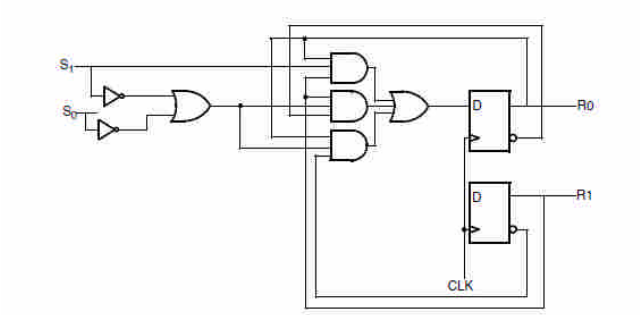
$S1\cdot\overline{S0}: R0 \leftarrow \overline{R0} \oplus \overline{R1}$

$S1\cdot S0: R0 \leftarrow R0 \wedge R1$

Find optimum logic using AND, OR, and NOT gates for the *D* input to the *D* flip-flop in the cell.

Answer:

設計過程可以斟酌給分



6. (20%) Design a counter that has a repeated sequence of six states as listed in following table.

Present State			Next State		
A	B	C	DA = A(t+1)	DB = B(t+1)	DC= C(t+1)
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	0	0	0

Answer:

$$D_A = A \oplus B$$

$$D_B = C$$

$$D_C = \overline{B}\,\overline{C}$$

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