CHAPTER 9

9-1.

$\log_2 64 = 6$ lines/mux or decoder

9-2.*

$C = C_8$

$V = C_8 \oplus C_7$

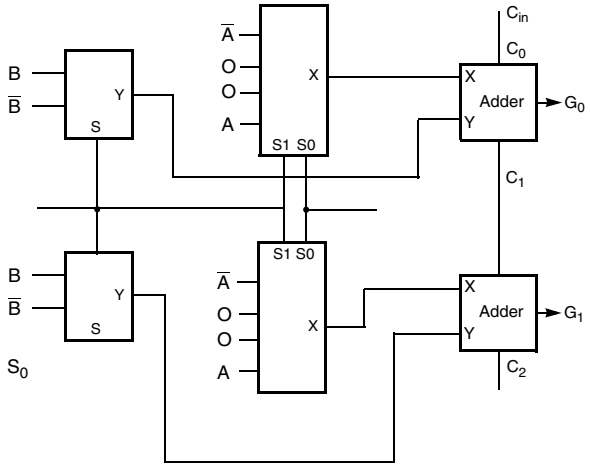
$Z = \overline{F_7 + F_6 + F_5 + F_4 + F_3 + F_2 + F_1 + F_0}$

$N = F_7$

9-3.*

$X = \overline{S}_1\overline{S}_0\overline{A} + S_0S_1A$

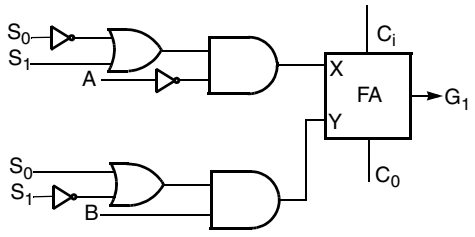
$Y = \overline{S}_1 B + S_1 \overline{B}$



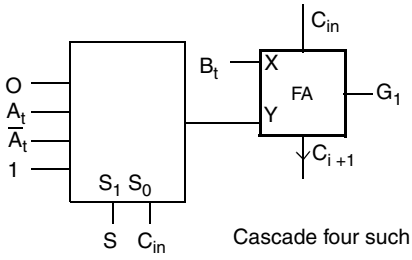
9-4.* (Errata: Delete "1" after problem number)

$X = \overline{A}\,S_1 + \overline{A}\,\overline{S}_1\,\overline{S}_0 = \overline{A}\,(S_1 + \overline{S}_1\,\overline{S}_0) = \overline{A}\,(S_1 + \overline{S}_0)$

$Y = S_1B + S_0\,S_1,\ B = B\,(\overline{S}_1 + S_0)$



9-5.



00: G = B

01: G = A + B

10: G = $\overline{A}$ + B

11: G = $\overline{B}$

Cascade four such stages, connecting the carries.

9-6.*

Two bits : The XOR, XNOR, NOR and AND are all bitwise operations. The design for one stage remains the same as any other Stages.

a) XOR = 00, NAND = 01, NOR = 10 XNOR = 11

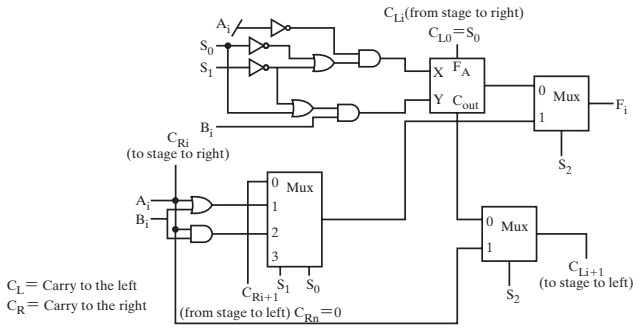
$\text{Out} = S_1 \overline{A}\,\overline{B} + \overline{S}_1 A\overline{B} + \overline{S}_1 \overline{A} B + S_1 S_0 AB + \overline{S}_1 S_0 \overline{A}$

b) The above is a simplest expression.

9-7.+

Logic table

S2	S1	S0	Operation
0	0	0	A + B
0	0	1	A + B + 1
0	1	0	$\overline{A}$
0	1	1	B + 1
1	0	0	Sr A
1	0	1	A v B
1	1	0	S l A
1	1	1	A ^ B



9-8.*

(a) 1001 (b) 0111 (c) 0101 (d) 0010

9-9.

	DA			AA			BA			MB	FS				MD	RW
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(a)	1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	1
(b)	1	0	1	-	-	-	1	1	1	0	1	1	1	0	0	1
(c)	1	0	1	-	-	-	-	-	-	-	-	-	-	-	1	1
(d)	1	0	0	-	-	-	1	0	0	0	1	1	0	1	0	1
(e)	0	1	1	0	0	1	-	-	-	1	0	1	0	1	0	1
(f)	0	1	0	0	1	0	-	-	-	-	0	0	0	1	0	1
(g)	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	1
(h)	0	1	1	1	0	0	1	0	1	0	0	0	1	0	0	1

9-10.*

(a)	$R5 \leftarrow R4 \wedge \overline{R5}$	R5 = 0000 0100	(d)	$R5 \leftarrow R0$	R5 = 0000 0000
(b)	$R6 \leftarrow R2 + \overline{R4} + 1$	R6 = 1111 1110	(e)	$R4 \leftarrow sr$Constant	R4 = 0000 0011
(c)	$R5 \leftarrow R0$	R5 = 0000 0000	(f)	$R3 \leftarrow$ Data in	R3 = 0001 1011

9-11.

$R3 \leftarrow R3 + R1, R3 = 01100111$ $R1 \leftarrow R1 + 1, R1 = 1100000$

$R4 \leftarrow R4 \vee R1, R4 = 01110100$ $R6 \leftarrow R6 + \overline{R1} + 1, R6 = 01100001$

$R5 \leftarrow R5 \oplus R1, R5 = 01101100$ $R7 \leftarrow R7 + \overline{R1} + 1, R7 = 01101001$

$R1 \leftarrow \overline{R1}, R1 = 11011111$ $R1 \leftarrow R7, R1 = 01101001$

R1 ... R7 = i, D, g, t, l, a, i Unscrambled is Digital

9-12.

a) 64 x 64 = 4096 b) 32 c) 0 to 4294967295 d) –2147483648 to +2147483647
errata : bit 31 as the sign bit makes sense

9-13.*

a) 8 bits b) 49 bits

9-14.

4 + 16 + 128 = 148

9-15.

Instruction Register Transfer	DA	AA	BA	MB	FS	MD	RW	MW	PL	JB
$R[0] \leftarrow R[7] \oplus R[3]$	000	111	011	0	1010	0	1	0	0	x
$R[1] \leftarrow M[R[4]]$	001	100	xxx	x	xxxx	1	1	0	0	x
$R[2] \leftarrow R[5] + 2$	010	101	xxx	1	0010	0	1	0	0	x
$R[3] \leftarrow$ sl $R[6]$	011	xxx	110	0	1110	0	1	0	0	x
if $R[4] = 0$ then $PC \leftarrow PC +$ se PC	xxx	100	xxx	x	0000	x	0	0	1	0

Instruction Register Transfer	Operation Code	DR	SA	SB or Operand
$R[0] =$ sr $R[7]$	000 1101	000	000	111
$R[1] \leftarrow M[R[6]]$	001 0000	001	110	000
$R[2] \leftarrow R[5] + 4$	100 0010	010	101	0100
$R[3] \leftarrow R[4] \oplus R[3]$	000 1010	011	100	011
$R[4] \leftarrow R[2] - R[1]$	000 0101	100	010	001

9-16.

MB: B15 - Correct for table specification

MD: B13 - Correct for table specification

RW:$\overline{B14}$ - Correct for table specification

MW: $\overline{B15}$ B14 - Correct for table specification

PL: B15 B14 - Correct for table specification

JB: B13 - Correct for table specification

BC: B9 - Correct for table specification

FS: The logic gives 0000 for FS for PL =1 which selects the value on the A input to the Function Unit to be evaluated for branches and blocks the value on bit 9 which is otherwise used as BC for branches. For PL = 0, the normal bits for FS are passed as required from the op code. Correct.

9-17.

Instruction	**Code**	**Registers/Memory changed**
ADD R0, R1, R2	000 0101 000 001 010	
SUB R3, R4, R5	000 001 011 100 101	R0 = 3
SUB R6, R7, R0	000 0101 110 111 000	R3 = -1
ADD R0, R0, R3	000 0101 000 000 011	R6 = 4
SUB R0, R0, R6	000 0101 000 000 110	R0 = 2
ST R7, R0	010 0000 000 111 000	R0 = -2
LD R7, R6	011 0000 111 110 000	M[7] = -2
ADI R0, R6, 2	100 0010 000 110 000	R7 = M[4]
ADI R3, R6, 3	100 0010 011 110 011	R0 = 6
		R3 = 7

9-18.

$$R[4] \leftarrow R[4] \oplus R[4]$$

V and C are produced by the arithmetic circuit. For the XOR FS code, S1 = 0, S0 = 1. and Cin = 0, giving arithmetic operation Add. For arbitrary contents in R[4], the values of C and V are a function of the sign and value of the contents of R4 and are unpredicable.

9-19.

Part	State	Opcode	VCNZ	Next State	IL	PS	DX	AX	BX	MB	FS	MD	RW	MM	MW
(a)	EX0	0000101	xxxx	EX1	0	01	0xxx	0xxx	0xxx	0	0101	0	1	0	0
(b)	EX0	0001101	xxxx	INF	0	01	1000	xxxx	1000	0	1101	0	1	0	0
(c)	EX0	1100000	xxx0	INF	0	10	xxxx	0xxx	xxxx	x	0000	0	0	0	0
	EX0	1100000	xxx1	INF	0	01	xxxx	0xxx	xxxx	x	0000	0	0	0	0
(d)	EX0	0000000	xxxx	INF	0	01	0xxx	0xxx	xxxx	x	0000	0	1	0	0

9-20.

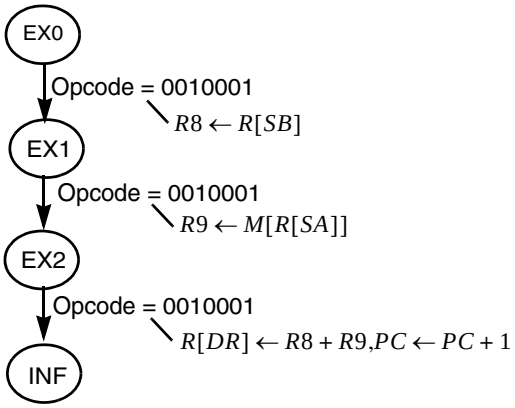
State	Instruction	R8	R9	Z	Next State
EX0	$R8 \leftarrow R[SA]$			0	EX1
EX1	$R9 \leftarrow zfOP$	0101100111000111	x	0	EX2
EX2	$R8 \leftarrow srR8$	0101100111000111	5	0	EX3
EX3	$R9 \leftarrow R9 - 1$	0010110011100011	5	0	EX2
EX2	$R8 \leftarrow srR8$	0010110011100011	4	0	EX3
EX3	$R9 \leftarrow R9 - 1$	0001011001110001	4	0	EX2
EX2	$R8 \leftarrow srR8$	0001011001110001	3	0	EX3
EX3	$R9 \leftarrow R9 - 1$	0000101100111000	3	0	EX2
EX2	$R8 \leftarrow srR8$	0000101100111000	2	0	EX3
EX3	$R9 \leftarrow R9 - 1$	0000010110011100	2	0	EX2
EX2	$R8 \leftarrow srR8$	0000010110011100	1	0	EX3
EX3	$R9 \leftarrow R9 - 1$	0000001011001110	1	1	EX4
EX4	$R[DR] \leftarrow R8$	0000001011001110	0	0	INF
INF	-	0000001011001110	0	-	-

9-21.+

Removal of the two decisions on zero operations does not affect the number of states in the state machine diagram. The reason for this is that the same states are required because the datapath of the computer only supports one register transfer per clock cycle. The transfers required by the instruction execution force the state structure. As a consequence, there can be no reduction of the number of clock cycles required to execute the instructions. The new state machine diagram is actually a worst case in terms of execution time for the instruction execution. The two decisions can only improve the execution times. So the analysis suggested is unnecessary.

9-22.

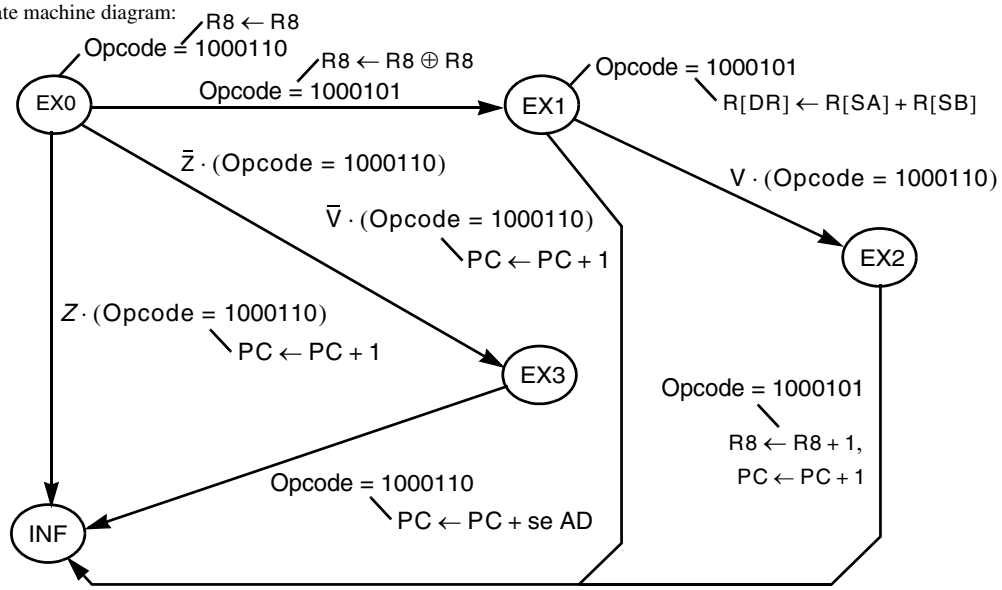
Partial state machine diagram:



State	Opcode	VCNZ	Next State	IL	PS	DX	AX	BX	MB	FS	MD	RW	MM	MW
EX0	0010001	xxxx	EX1	0	00	1000	xxxx	0xxx	0	1100	0	1	0	0
EX1	0010001	xxxx	EX2	0	00	1001	0xxx	xxxx	x	xxxx	1	1	0	0
EX2	0010001	xxxx	INF	0	01	0xxx	1000	1001	0	0010	1	0	0	0

9-23.

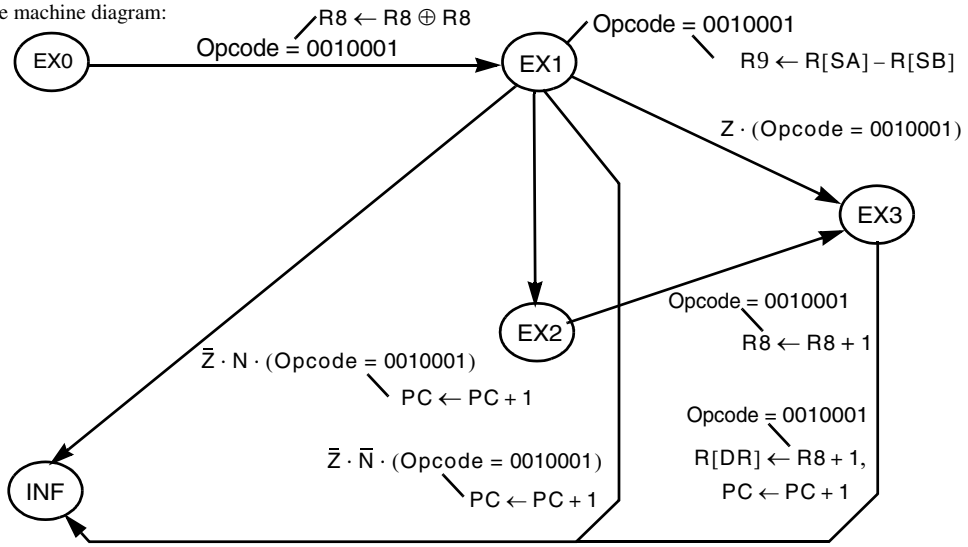
Partial state machine diagram:



Part	State	Opcode	VCNZ	Next State	IL	PS	DX	AX	BX	MB	FS	MD	RW	MM	MW
AOV	EX0	1000101	xxxx	EX1	0	00	0xxx	1000	1000	0	1010	0	1	x	0
	EX1	1000101	1xxx	EX2	0	00	0xxx	0xxx	0xxx	0	0010	0	1	x	0
	EX1	1000101	0xxx	INF	0	01	0xxx	0xxx	0xxx	0	0010	0	1	x	
	EX2	1000101	xxxx	INF	0	01	1000	1000	xxxx	0	0001	0	1	x	0
BRV	EX0	1000110	xxx0	EX3	0	00	1000	1000	xxxx	x	0000	0	1	x	0
	EX0	1000110	xxx1	INF	0	01	1000	1000	xxxx	x	0000	0	1	x	0
	EX3	1000110	xxxx	INF	0	10	xxxx	xxxx	xxxx	x	xxxx	0	0	x	0

9-24.

Partial state machine diagram:



State	Opcode	VCNZ	Next State	IL	PS	DX	AX	BX	MB	FS	MD	RW	MM	MW
EX0	0010001	xxxx	EX1	0	00	1000	1000	1000	0	1010	0	1	0	0
EX1	0010001	xxx1	EX3	0	00	1001	0xxx	0xxx	0	0101	0	1	0	0
EX1	0010001	xx00	EX2	0	00	1001	0xxx	0xxx	0	0101	0	1	0	0
EX1	0010001	xx10	INF	0	01	1001	0xxx	0xxx	0	0101	0	1	0	0
EX2	0010001	xxxx	EX3		00	1000	1000	xxxx	x	0001	0	1	0	0
EX3	0010001	xxxx	INF	0	01	0xxx	1000	xxxx	x	0001	0	1	0	0

9-25.+ (Errata: Add a + and the following hint. "Hint: In order to address all eight registers, it is necessary to provide eight values for SB in the Instruction Register. Since the instruction register can only be loaded from memory, these "instructions" must be placed in memory temporarily during the instruction execution and loaded into the IR as data without using the normal instruction fetch.")

The operation code used for SMR and these instructions is 0111111 which is easy to generate by complementing all 0's. The word to be stored in memory is built in a register by complementing all 0's and ANDing the result with the value of SB from the original instruction. The register value generated is incremented, stored in memory and loaded into the IR after the execution of each transfer from a register to a memory location.

Register Transfer	State	Opcode	VCNZ	Next State	IL	PS	DX	AX	BX	MB	FS	MD	RW	MM	MW
R8 ← R[SA]	EX0	0111111	xxxx	EX1	0	00	1000	0xxx	xxxx	0	0000	1	1	0	0
R9 ← R9 ⊕ R9 (R9 ← 0)	EX1	0111111	xxxx	EX2	0	0	1001	1001	1001	0	1010	0	1	0	0
R9 ← $\overline{R9}$	EX2	0111111	xxxx	EX3	0	0	1001	1001	xxxx	x	1011	0	1	0	0
R10 ← sr R9	EX3	0111111	xxxx	EX4	0	0	1010	1001	xxxx	x	1101	0	0	0	0
R9 ← R10 ∧ zf SB	EX4	0111111	xxxx	EX5	0	0	1001	1010	xxxx	1	1000	0	1	0	0
R11 ← zf SB	EX5	0111111	xxxx	EX6	0	0	1011	xxxx	xxxx	1	1100	0	1	0	0
M[R10] ← R9	EX6	0111111	xxxx	EX7	0	0	xxxx	1010	1001	0	xxxx	x	0	0	1
IR ← M[R10]	EX7	0111111	xxxx	EX8	1	0	xxxx	1010	xxxx	x	xxxx	x	0	0	0
M[R8] ← R[SB]	EX8	0111111	xxxx	EX9	0	0	xxxx	1000	0xxx	0	xxxx	1	1	0	0
R8 ← R8 + 1	EX9	0111111	xxxx	EX10	0	0	1000	1000	xxxx	x	0001	0	1	0	0
R9 ← R9 + 1	EX10	0111111	xxxx	EX11	0	0	1001	1001	xxxx	x	0001	0	1	0	0
R11 ← zf SB, $\overline{Z}$: → EX5	EX11	0111111	xxx0	EX5	0	0	xxxx	1011	xxxx	1	0101	x	0	0	0
R11 ← zf SB, Z : → INF, inc PC	EX11	0111111	xxx1	INF	0	01	xxxx	1011	xxxx	1	0101	x	0	0	0

9-26. (Errata: Solution of this problem with the architecture available is too difficult and while it can be solved, any solution is highly impractical. It will be removed in the 2nd and subsequent printings.)