CSA051 - Digital Systems

數位系統導論

Chapter 6
Registers and Counters

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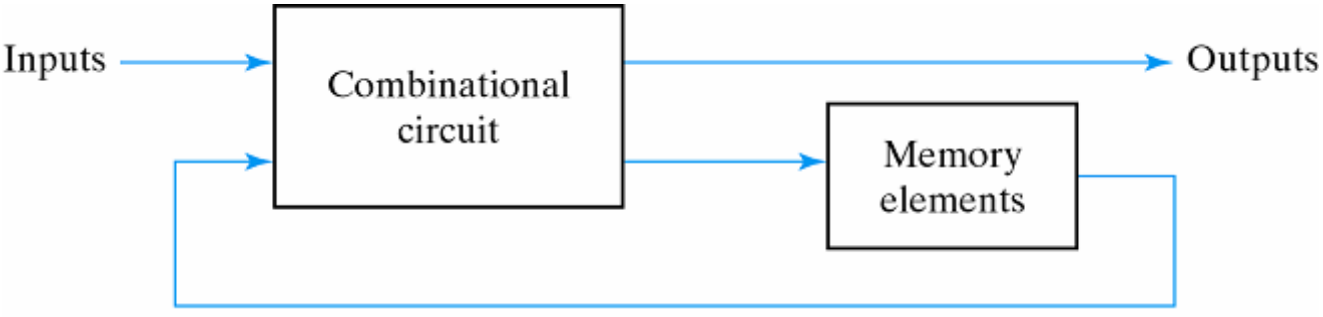
Chapter 6 Registers and Counters

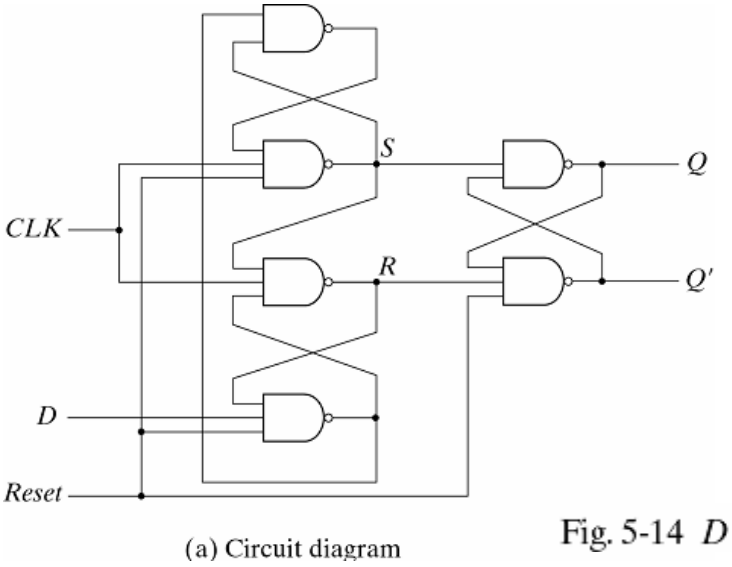
6-1 Registers



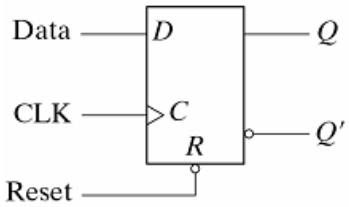
- Clocked sequential circuit
  - No flip-flops / no feedbacks → reduce to combinational circuit
  - No combinational circuit → remain a sequential circuit
    - registers and counters
- Register: a group of flip-flops capable of storing one bit of information
  - n-bit register consists of a group of n flip-flops capable of storing n bits
- Counter: a register going through a predetermined sequence of states

4-bit Register

- Simplest register: consisting of only flip-flops without any gates
- Example 6-1: 4-bit register
  - positive edge trigger
  - When the clear input goes to 0, all flip-flops are reset
  - The R inputs must be maintained at logic 1 during normal clocked operation



(a) Circuit diagram



(b) Graphic symbol

R	C	D	Q	Q′
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(c) Function table

Fig. 5-14 *D* Flip-Flop with Asynchronous Reset

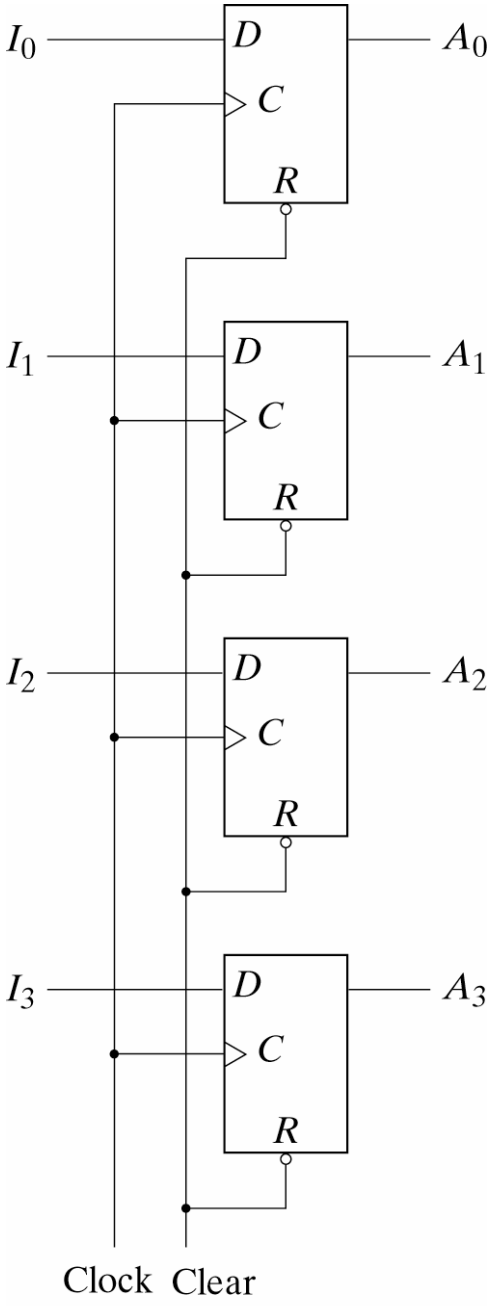


Fig. 6-1 4-Bit Register

Register with Parallel Load

Parallel load

- loading: the transfer of new information into a register
- parallel loading: all the bits of the register are loaded simultaneously with a common clock pulse
  - ***Load control***: determine when to load new information

Approaches to register with parallel load

1. controlling the *clock input signal* with an enabling gate: uneven propagation delays between the master clock and the inputs of flip-flops
2. controlling the *D inputs*: ensure that all clock pulses arrive at the same time anywhere in the system

4-bit register with a load control input

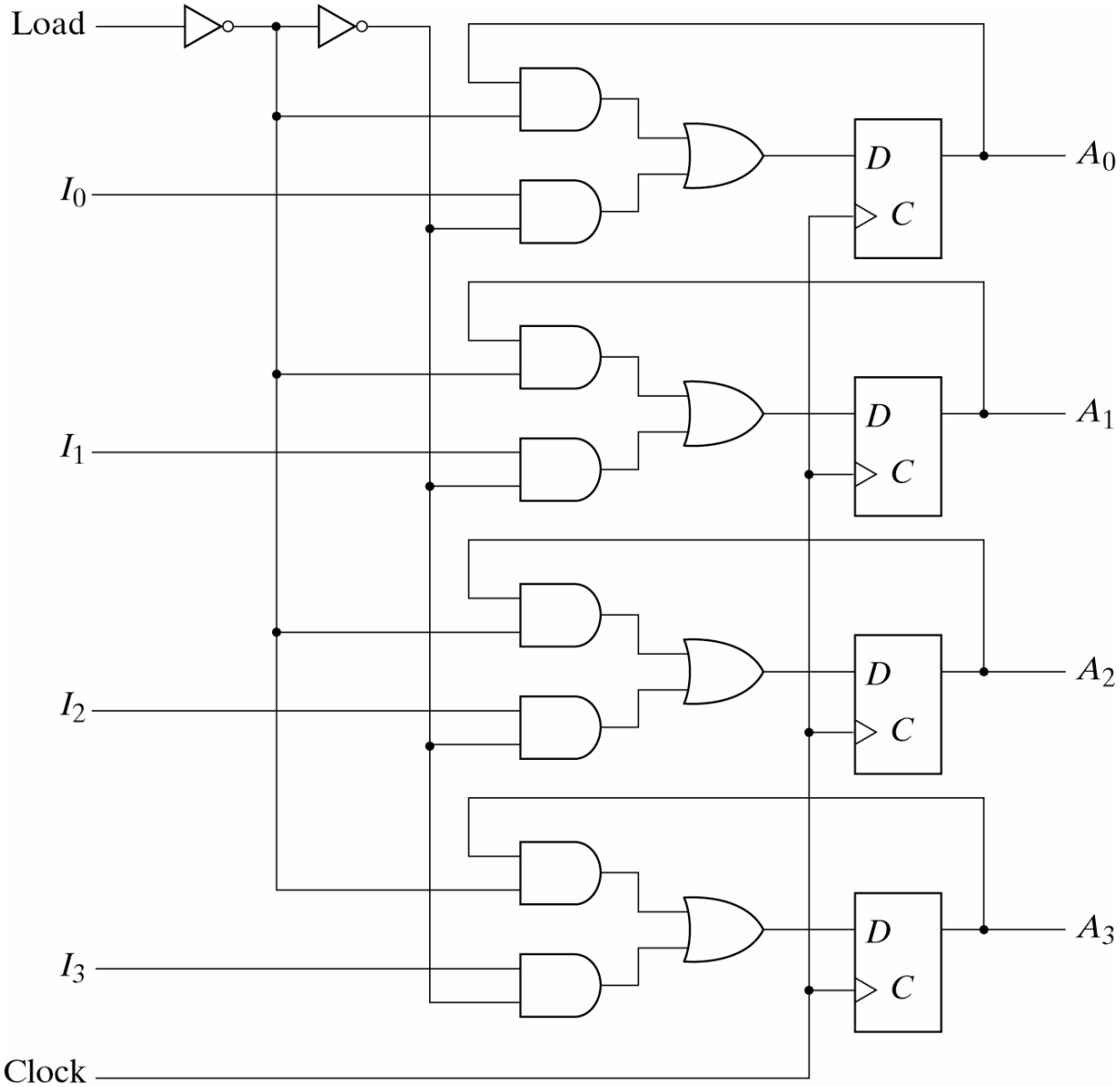


Fig. 6-2 4-Bit Register with Parallel Load

load=1

- data are transferred into the register with the next positive edge of the lock

load=0

- outputs are connected to their respective inputs

- The feedback connection is necessary because the D flip-flop does not have a "no change" condition
- The clock pulses are applied to the C inputs at all times

6-2 Shift Registers

- shift register: a register capable of shifting its binary information in one or both directions
- Example Fig. 6-3: each clock pulse shifts the contents of the register one bit position to the right
  - serial input: determines what goes into the leftmost flip-flop
  - serial output: taken from the output of the rightmost flip-flop
- ***Shift control***: make the shift occur only with certain pulses
  - inhibiting the clock
  - control through the D inputs (shown later)

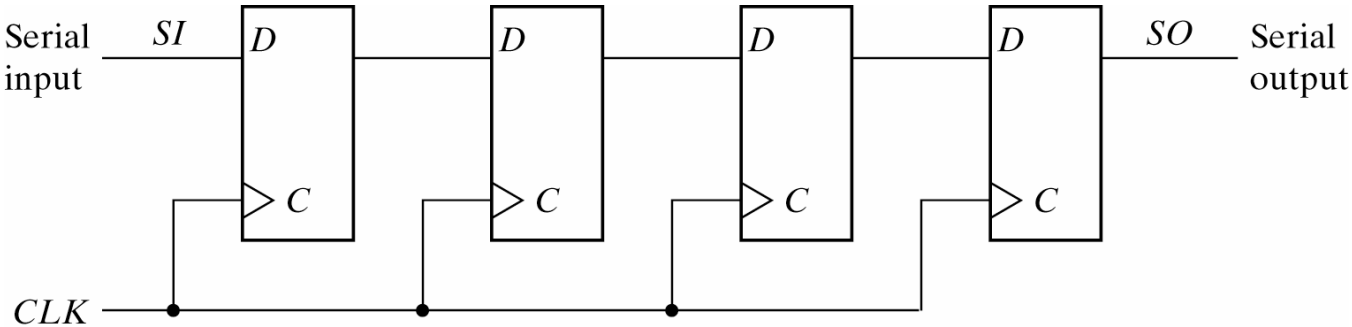
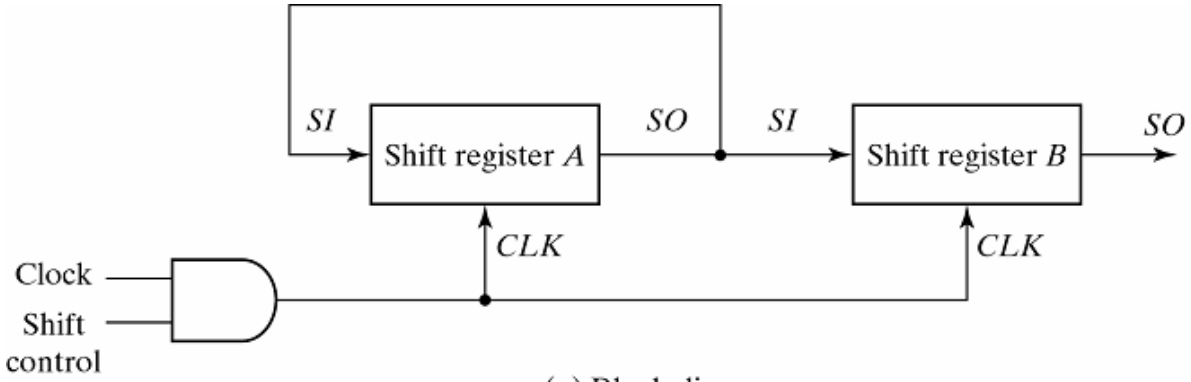


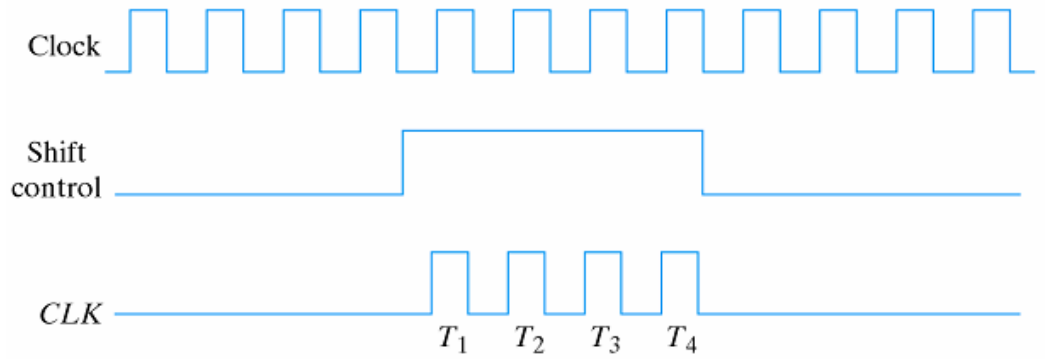
Fig. 6-3 4-Bit Shift Register

Serial Transfer

serial transfer: information is transferred one bit at a time by shifting the bits out of source register into destination register



(a) Block diagram



(b) Timing diagram

Fig. 6-4 Serial Transfer from Register *A* to register *B*

- The serial output (SO) of register A is connected to the serial input (SI) of register B and the SI of register A itself
- The shift control input determines when and how many times the registers are shifted
- serial vs. parallel

Table 6-1
Serial-Transfer Example

Timing Pulse	Register *A*	Register *B*
Initial value	1 0 1 1	0 0 1 0
After T_1	1 1 0 1	1 0 0 1
After T_2	1 1 1 0	1 1 0 0
After T_3	0 1 1 1	0 1 1 0
After T_4	1 0 1 1	1 0 1 1

Serial Addition

Register A holds the augend and register B holds the addend

– Initially, register A and carry flip-flop are cleared to 0

All the numbers are transferred serially into B and added to A

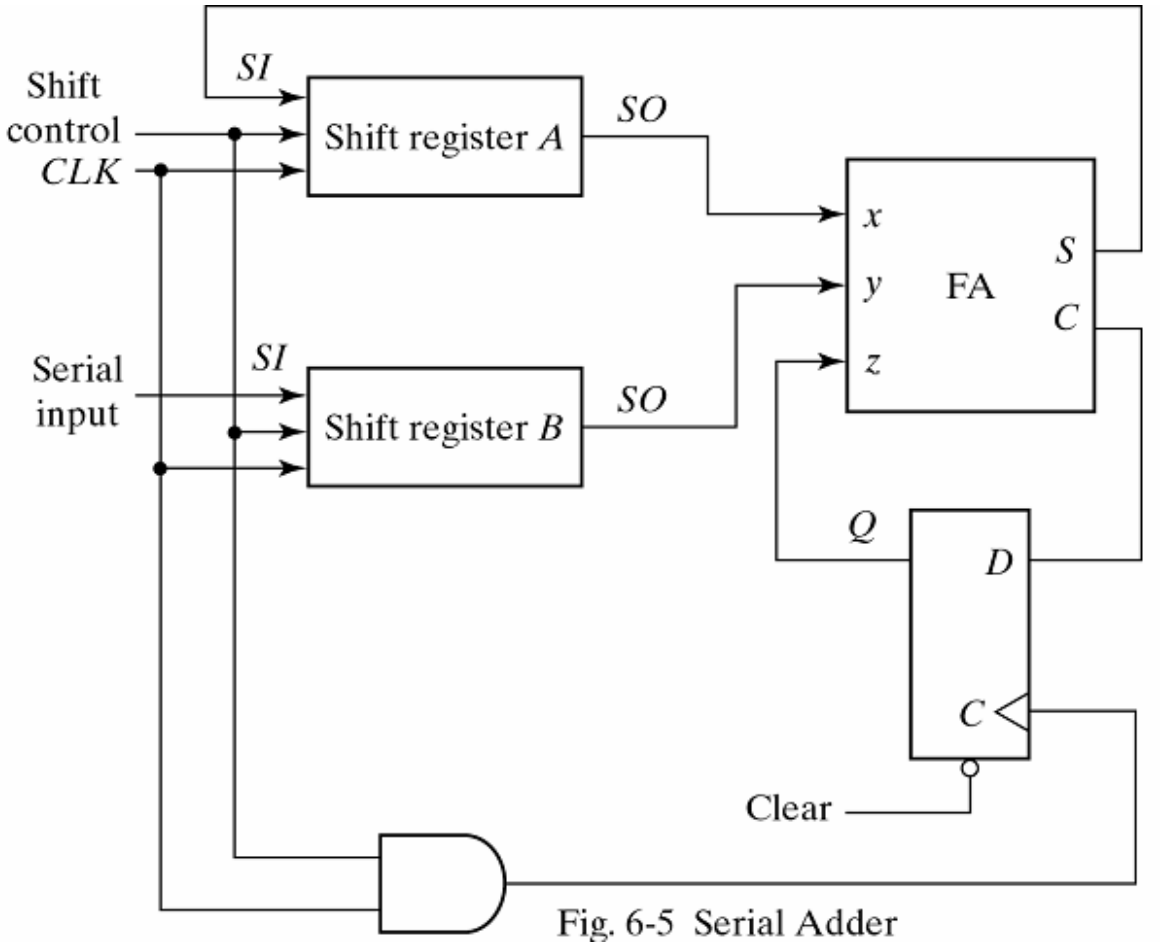


Fig. 6-5 Serial Adder

- parallel adder: use registers with parallel load
  - # of full adders = # of bits
  - faster
  - combinational circuit
- serial adder: use shift registers
  - requiring less equipment
  - only one full adder
  - sequential circuit

Second Form of Serial Adder

Table 6-2 *State Table for Serial Adder*

Present State	Inputs		Next State	Output	Flip-Flop Inputs	
Q	X	y	Q	S	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

Design a serial adder using a JK FF

- Assume 2 shift registers as input
- Obtain state table with FF input/outputs
- Obtain input and output equations
- Draw the circuit

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

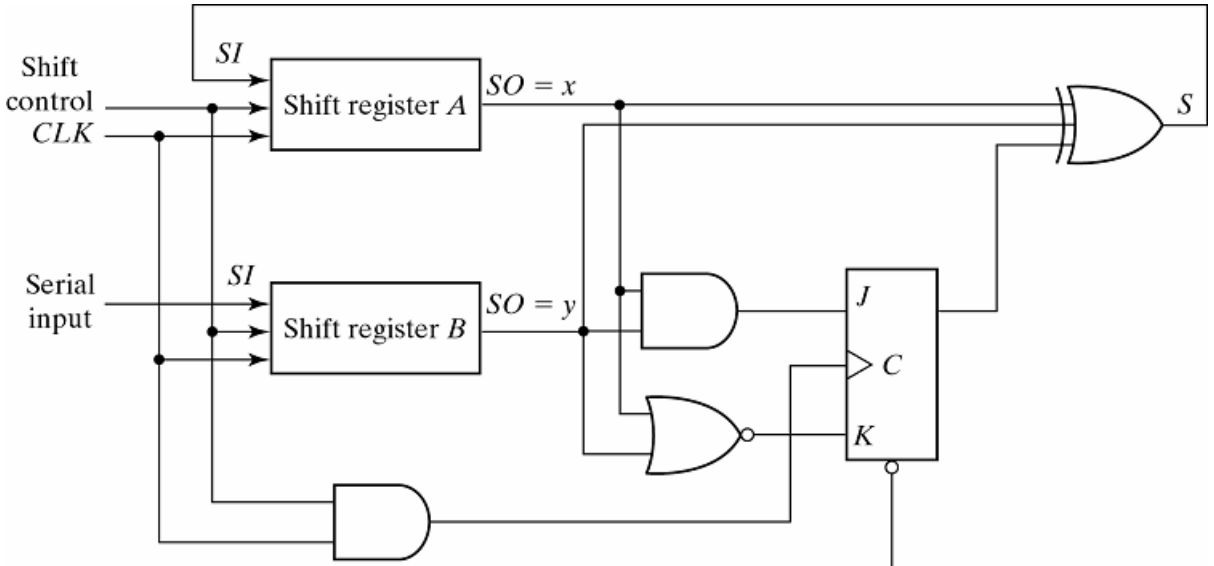


Fig. 6-6 Second form of Serial Adder

$$J_Q = xy$$
$$K_Q = x'y' = (x + y)'$$
$$S = x \oplus y \oplus Q$$

no full-adder

Universal Shift Register

- Unidirectional shift register: capable of shifting in one direction only
- Bidirectional shift register: capable of shifting in both directions
- universal shift register: has both shifts and parallel load capabilities
- The most general shift register has the following capabilities:

1. A *clear* control to clear the register to 0.
2. A *clock* input to synchronize the operations.
3. A *shift-right* control to enable the shift right operation and the *serial input* and *output* lines associated with the shift right.
4. A *shift-left* control to enable the shift left operation and the *serial input* and *output* lines associated with the shift left.
5. A *parallel-load* control to enable a parallel transfer and the n input lines associated with the parallel transfer.
6. n parallel output lines.
7. A control state that leaves the information in the register unchanged in the presence of the clock.

4-bit Universal Shift Register

Has all the capabilities listed above

Selection inputs control the mode of operation

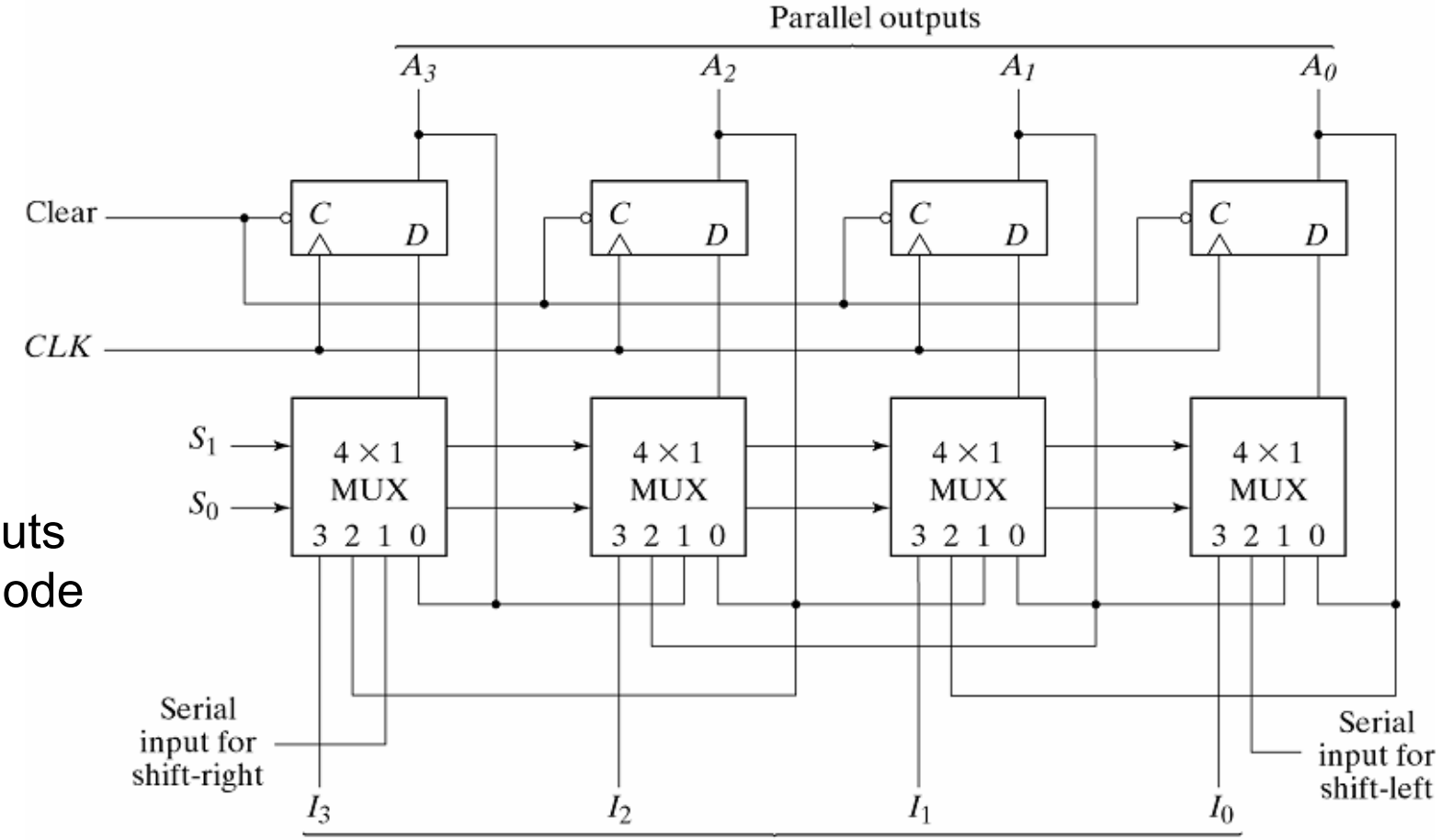


Fig. 6-7 4-Bit Universal Shift Register

Table 6-3 *Function Table for the Register of Fig. 6-7*

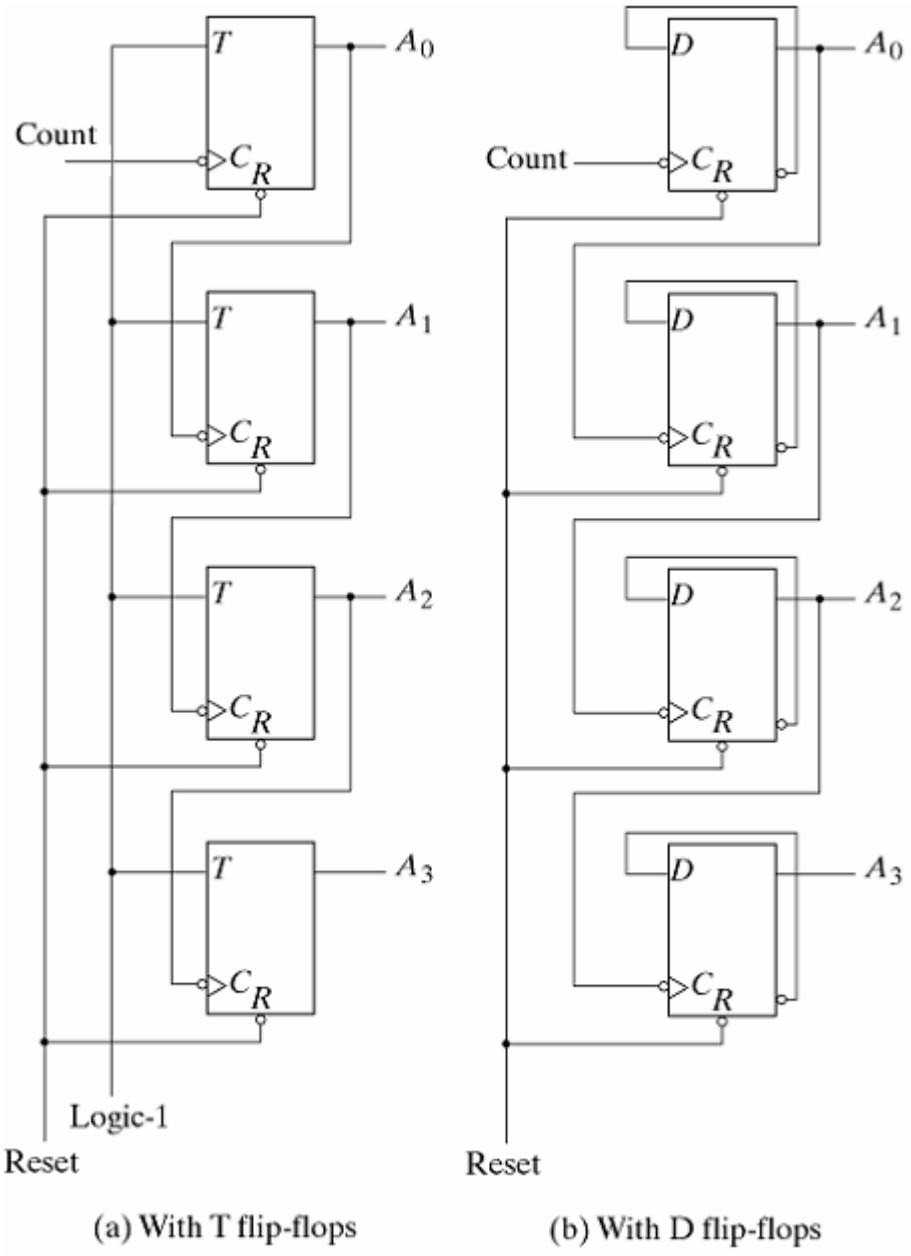
Mode Control			
S_1	S_0	Register Operation	
0	0	No change	Ai
0	1	Shift right	Ai+1
1	0	Shift left	Ai-1
1	1	Parallel load	Ii

Shift registers are often used to interface digital systems situated remotely from each other

6-3 Ripple Counters

- ***counter***: a register that goes through a prescribed sequence of states upon the application of input pulses
  - – may occur at a fixed interval of time or at random
  - – may follow the binary number sequence or any other sequence of states
  - – n-bit ***binary counter***: n flip-flops counting in binary from 0~2^n-1
- Two categories
  - – ***Ripple counters***: FF output transition serves as a source for triggering other via the clock pin
    - Binary ripple counter
    - BCD ripple counter
  - – ***Synchronous counters***: inputs of all FF receive the common clock
    - discussed in Sections 6-4 and 6-5

Figure 6-8 4-Bit Binary Ripple Counter



- One single count input
- Output of each FF connected to C input of next higher-order FF
- Three approaches
  - from T
  - from JK: J and K inputs tied together
  - from D: complement output connected to the D input

Binary Count Sequence

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

Every time A_i goes from 1 to 0, it complements A_{i+1} (Negative trigger)

A_3	A_2	A_1	A_0
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1

Binary count-down counter

- use positive-trigger T flip-flops instead

BCD Ripple Counter

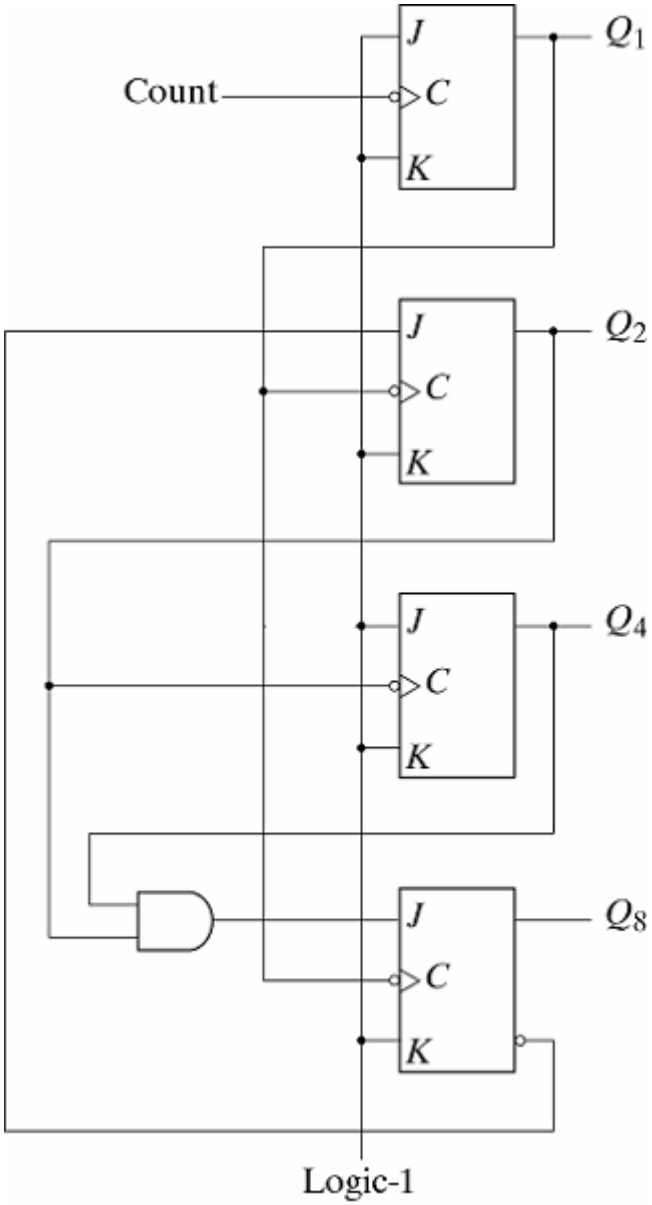


Fig. 6-10 BCD Ripple Counter

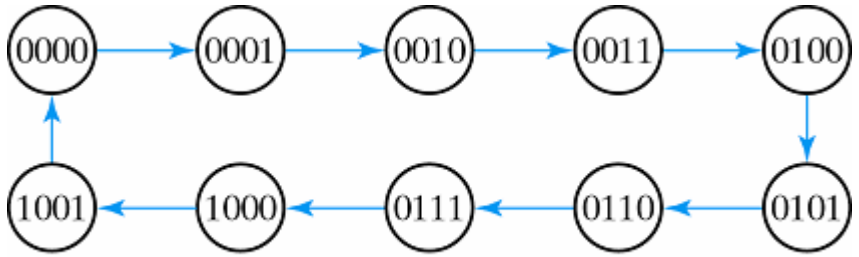


Fig. 6-9 State Diagram of a Decimal BCD-Counter

- Decade decimal counter: 0 ~ 9
- Need at least 4 flip-flops, similar to a binary counter, but state after 1001 is 0000

Q_8	Q_4	Q_2	Q_1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
0	0	0	0

Q_1: count input
Q_2: Q_1 negative-edge and Q_8 = 0
Q_4: Q_2 negative-edge
Q_8: Q_1 negative-edge and Q_2=Q_4

J K	Q(t+1)	JK Flip-Flop
0 0	Q(t)	No change
0 1	0	Reset
1 0	1	Set
1 1	Q'(t)	Complement

Three-Decade Decimal BCD Counter

- n-decade counter: count from 0 to 10^n-1
- Input to n^{th} decades come from Q_8 of the previous $(n-1)^{th}$ decade
- When Q8 in one decade goes from 1 to 0, it triggers the count for the next higher-order decade while its own decade goes from 9 to 0

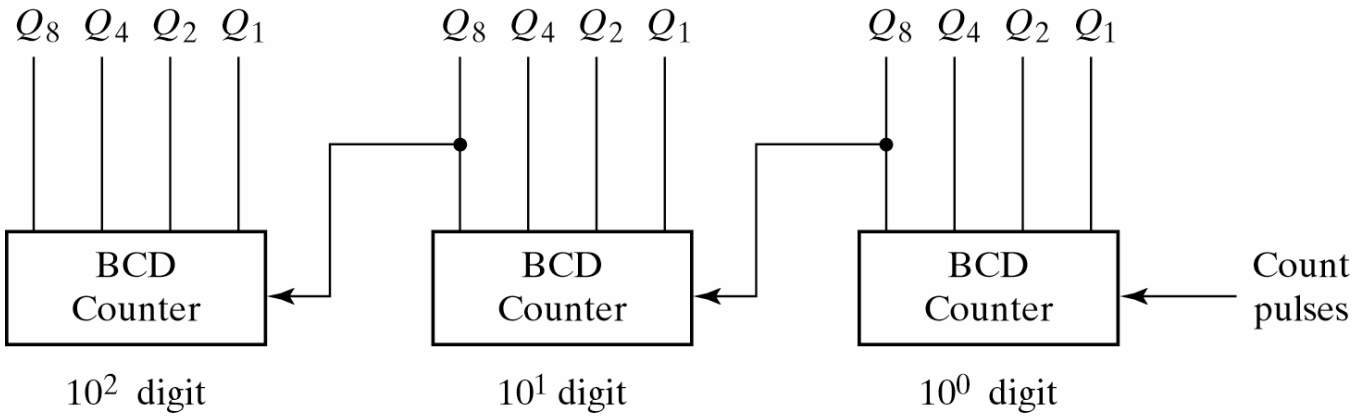


Fig. 6-11 Block Diagram of a Three-Decade Decimal BCD Counter

6-4 Synchronous Counters

- synchronous counter: clock pulses are applied to inputs of all FF
- 3-bit binary counter with T flip-flops

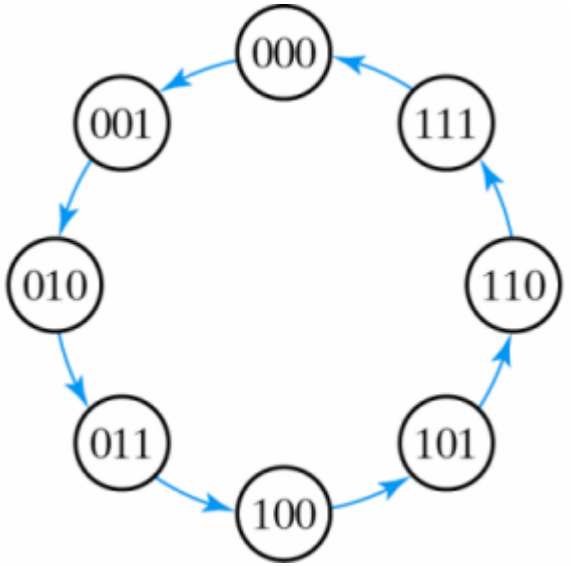


Fig. 5-29 State Diagram of 3-Bit Binary Counter

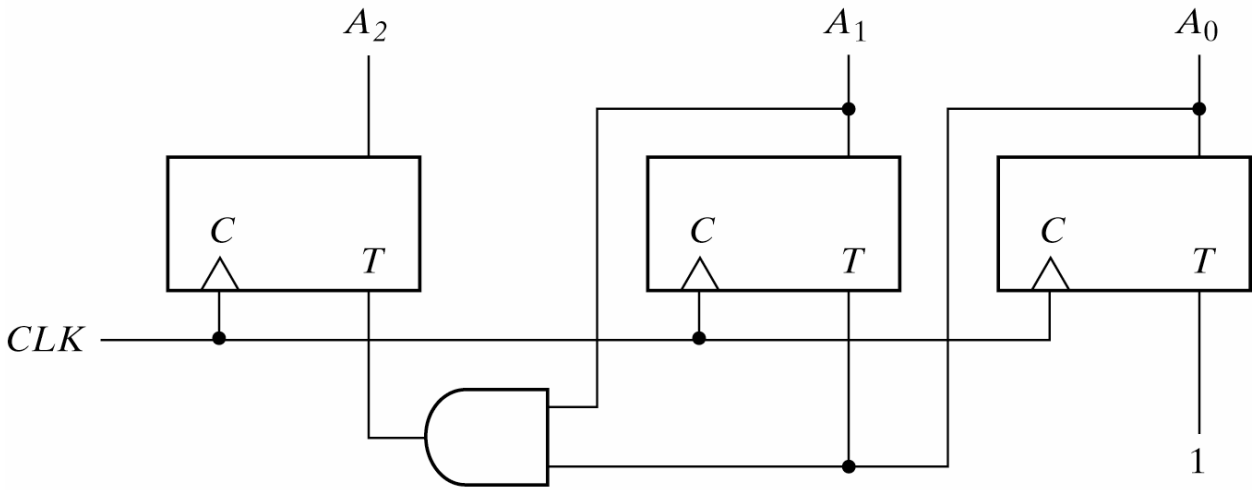
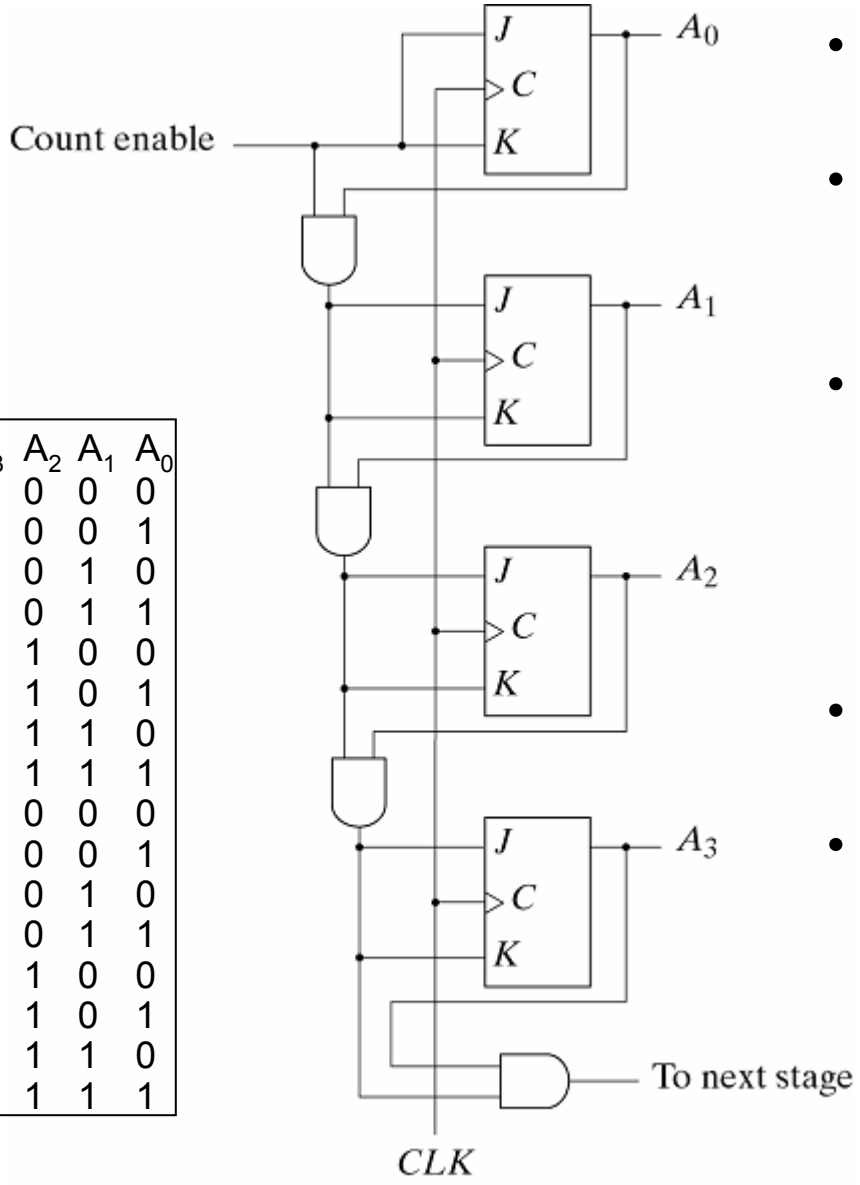


Fig. 5-31 Logic Diagram of 3-Bit Binary Counter

$T_{A2}=A_1A_0$ $T_{A1}=A_0$ $TA_0=1$

4-Bit Synchronous Binary Counter



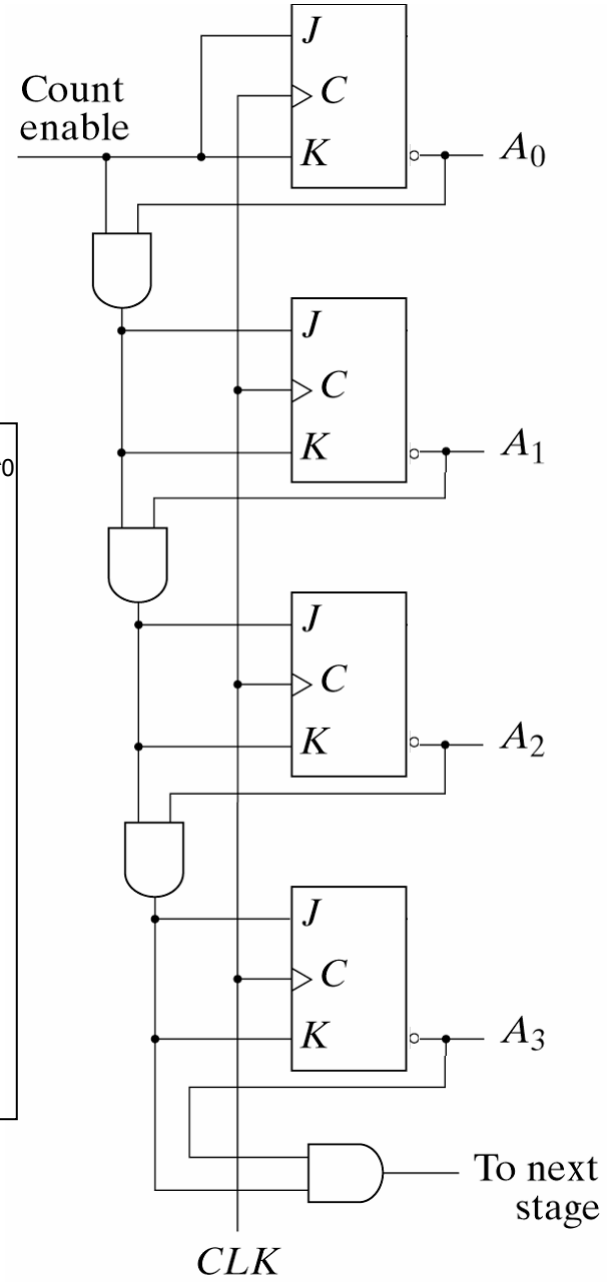
A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Fig. 6-12 4-Bit Synchronous Binary Counter

- least significant position: complemented with every pulse
- any other positions: complemented if all lower significant bits are **equal to 1**

- It can be extended to any number of stages, with each stage having an addition FF and an AND gate that gives the output of 1 if all previous FF outputs are 1
- It can be triggered with either the positive or the negative clock edge
- It can be either of the JK-type, the T-type, or the D-type with XOR gates

Synchronous Count Down Binary Counter



A_3	A_2	A_1	A_0
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0

- similar to 4-Bit synchronous count up binary counter
- least significant position: complemented with every pulse
- any other positions: complemented if all lower significant bits are **equal to 0**

Up-Down Binary Counter

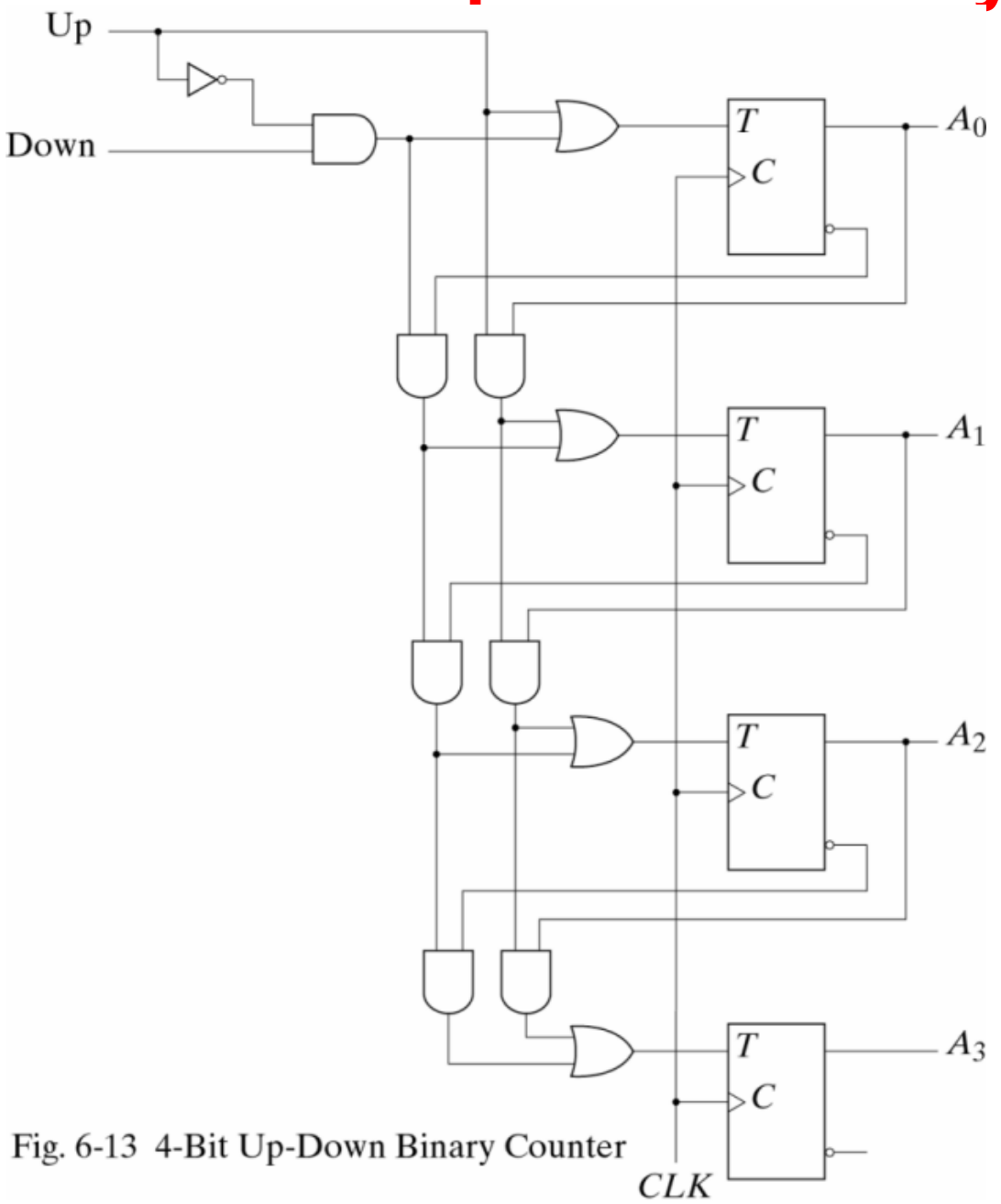


Fig. 6-13 4-Bit Up-Down Binary Counter

up	down	operation
1	x	count up
0	1	count down
0	0	no change

an up-down binary counter using T flip-flops

BCD Counter

count from 0000 to 1001 and back to 0000

Table 6-5 *State Table for BCD Counter*

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

minterms 10 to 15 are taken as don't-care terms

$$T_{Q1} = 1$$
$$T_{Q2} = Q_8' Q_1$$
$$T_{Q4} = Q_2 Q_1$$
$$T_{Q8} = Q_8 Q_1 + Q_4 Q_2 Q_1$$
$$y = Q_8 Q_1$$

4 T flip-flops, 5 AND gates, and 1 OR gate

Binary Counter with Parallel Load

Load an initial binary number into the counter prior to the count operation

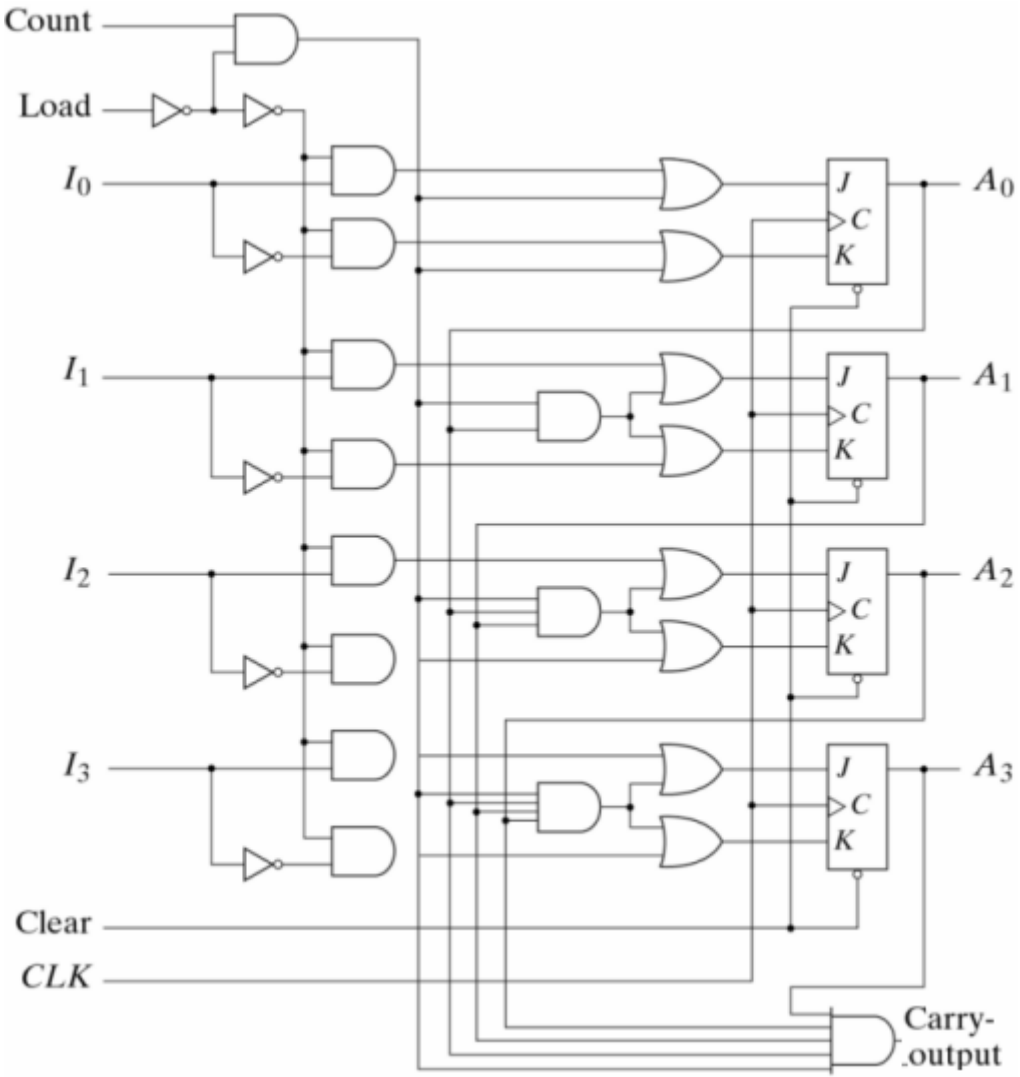


Fig. 6-14 4-Bit Binary Counter with Parallel Load

Table 6-6 *Function Table for the Counter of Fig. 6-14*

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

Table 5-1 *Flip-Flop Characteristic Tables*

***JK* Flip-Flop**

J	K	$Q(t+1)$	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

It can be used to generate any desired count sequence

A BCD Counter using a Binary Counter with Parallel Load

The AND detects the occurrence of state 1001 and then the counter reloads 0

The NAND detects the occurrence of state 1010 and then the counter is cleared to 0

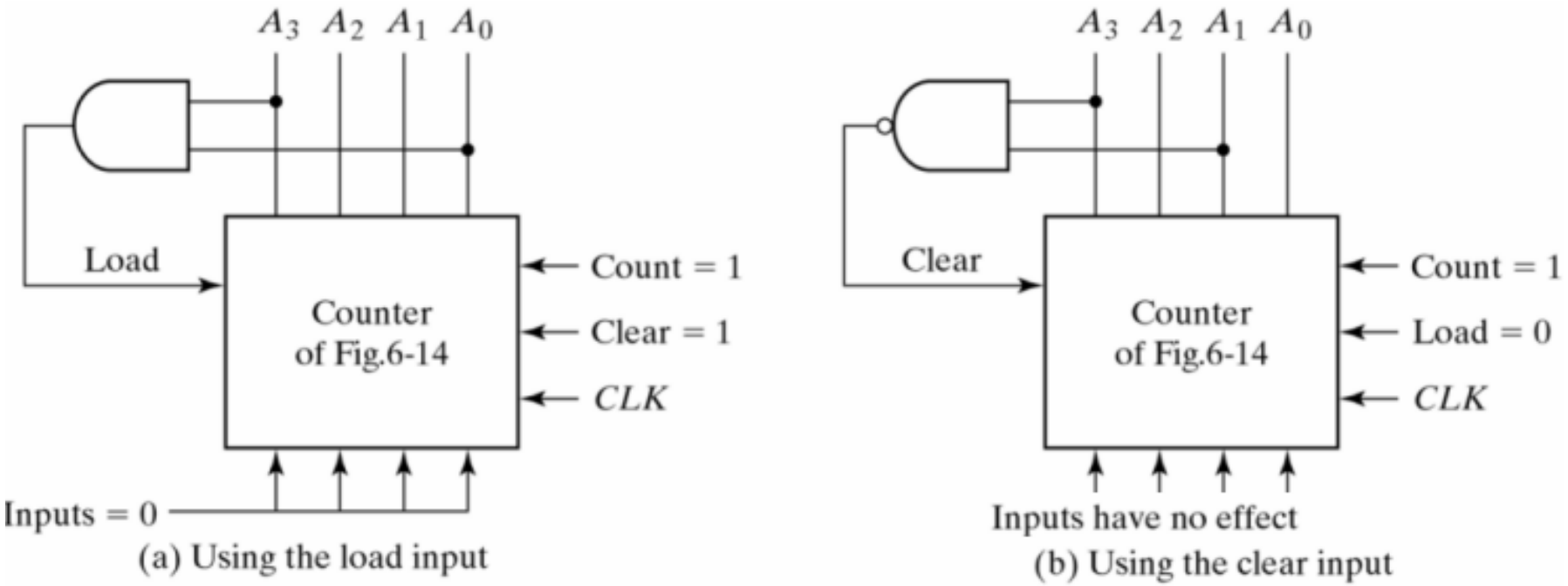


Fig. 6-15 Two ways to Achieve a BCD Counter Using a Counter with Parallel Load

6-5 Other Counters

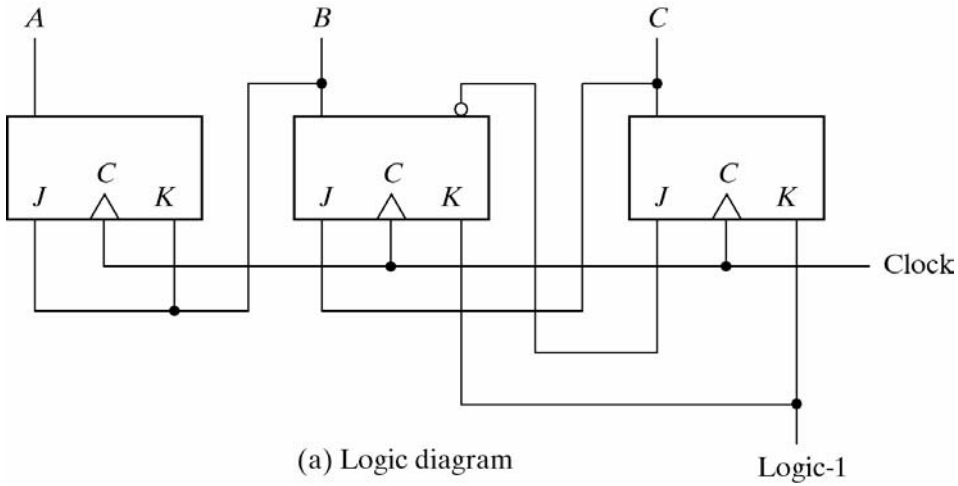
- Divide-by-N counter (modulo-N counter): a counter that goes through a repeated sequence of N states
- Counters can be used to generate timing signals to control the sequence of operations in a digital system
- Counters can be constructed also by means of shift registers
- The sequence of counters may follow the binary count or may be any other arbitrary sequence
- non-binary counters
  - Ring counter
  - Johnson counter

Counter with Unused States

- Outside interference may cause a circuit to enter one of the unused states
- Example:

Table 6-7 State Table for Counter

Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X



(a) Logic diagram

two unused states: 011 and 111

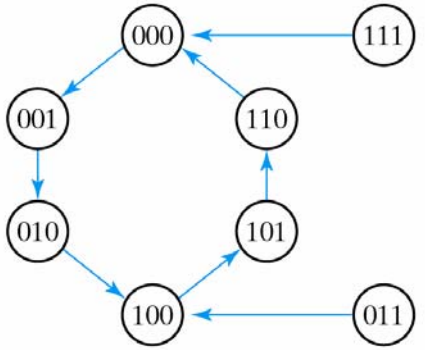
Simplified equations:

$J_A=B$ $K_A=B$

$J_B=C$ $K_B=1$

$J_C=B'$ $K_C=1$

We need to analyze the circuit to determine the effects of unused states!



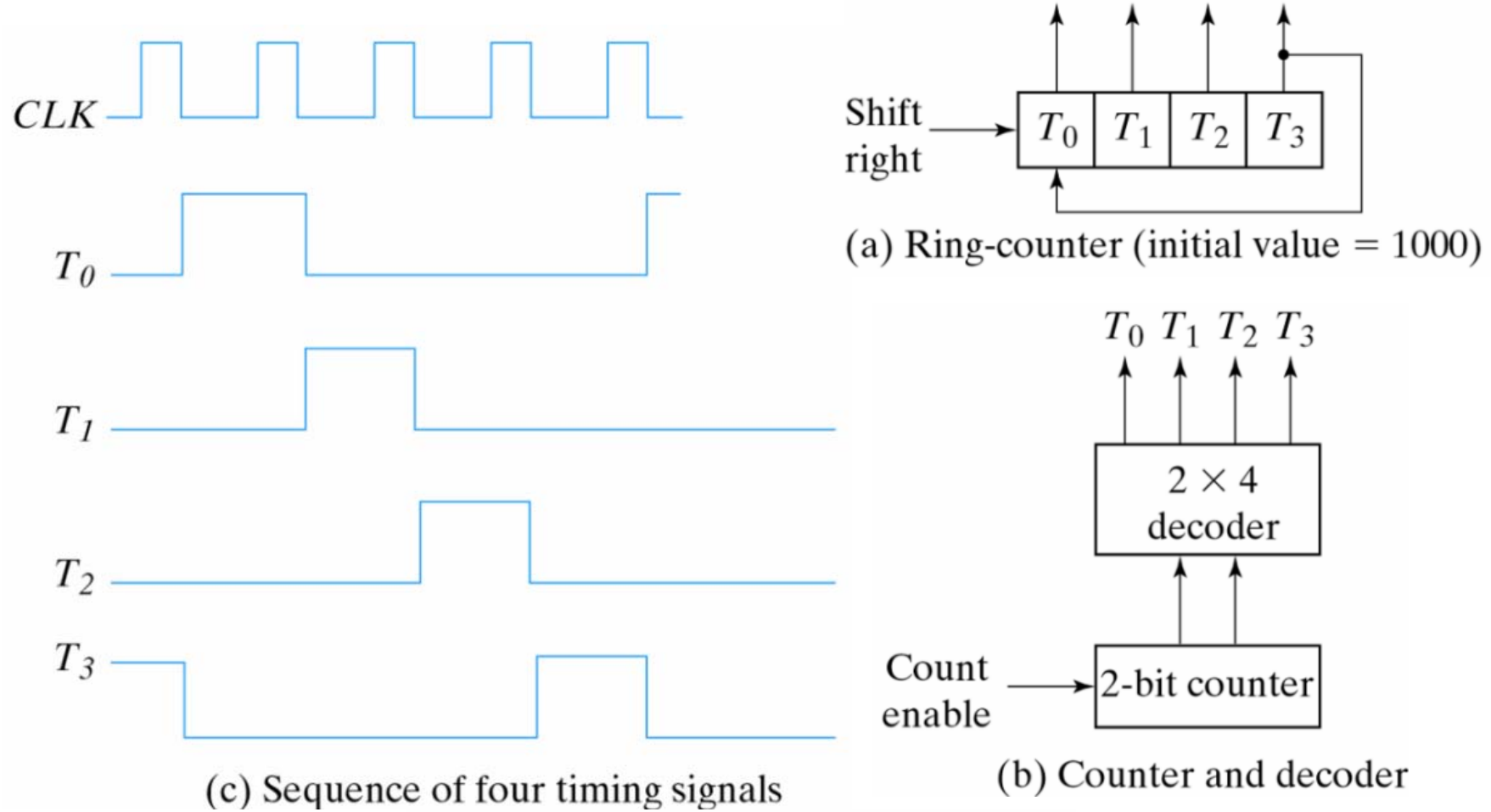
(b) State diagram

Fig. 6-16 Counter with Unused States

Self correcting counter: if it happens to be in an unused state, it eventually reaches the normal counter sequence after one or more clock pulses

Ring Counter

- ring counter: a circuit shift register with only one flip-flop being set an any particular time, all others are cleared. The single bit is shifted from one flip-flop to the next to produce the sequence of timing signals
- Two approaches: (a) ring-counter (b) counter and decoder
- k-bit ring counter: k flip-flops to provide k distinguishable states



(a) Ring-counter (initial value = 1000)

(b) Counter and decoder

(c) Sequence of four timing signals

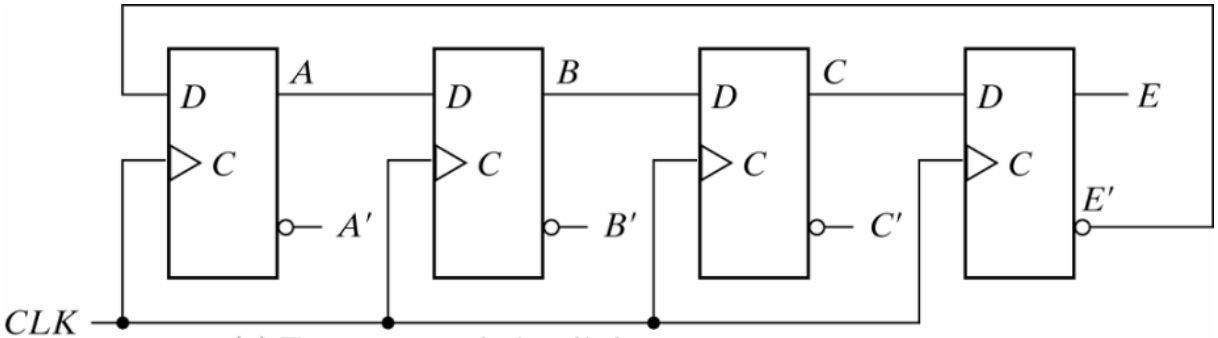
Fig. 6-17 Generation of Timing Signals

Johnson Counter

switch-tail ring counter: a circular shift register with the complement output of the last flip-flop connected to the input of the first flip-flop

– double the number of states for a ring counter (Figure 6-17a)

Johnson counter: a k-bit switch-tail counter with 2k decoding gates to provide outputs for 2k timing signals



(a) Four-stage switch-tail ring counter

Sequence number	Flip-flop outputs A	B	C	E	AND gate required for output
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

(b) Count sequence and required decoding

Fig. 6-18 Construction of a Johnson Counter

Connecting Figure 6-18a with 8 AND gates listed Figure 6-18b to complete the construction of the Johnson counter

- Disadvantage: it never finds its way to a valid state if it is at an unused state

  -Correcting: $D_C = (A+C)B$
- # of FF = ½ # of timing signals
- # of 2-input decoding gates = # of time signals

Summary

Chapter 6 Registers and Counters

6-1 Registers

4-bit register, register with parallel load

6-2 Shift Registers

4-bit shift register, serial shift register, serial adder, second-form serial adder, universal shift register

6-3 Ripple Counters

4-bit binary ripple counter, count-down counter, BCD ripple counter, multi-decade BCD counter

6-4 Synchronous Counters

4-bit synchronous binary counter, count-down counter, up-down binary counter, BCD counter, binary counter with parallel load

6-5 Other Counters

ring counter, Johnson counter